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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,050	06/26/2001	Harold Kutz	CYPR-CD00199	4196

7590 01/05/2005

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EXAMINER	
MASON, DONNA K	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,050	KUTZ ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cov r sh et with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 7-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Although claim 1 is identified as "previously *amended*", it should be noted that claim 1, as currently presented, includes added text (underlined) and deleted text (strikethroughs) that is identical to the added text and deleted text previously presented in the response filed on April 19, 2004.

Furthermore, "previously *amended*" (emphasis added) is not a permissible identifier. A claim that was previously amended in an earlier amendment paper should be indicated as "previously *presented*" (emphasis added).

Nonetheless, claim 1 has been treated as presented. Applicant is reminded of the revised amendment practice described in 37 CFR 1.121.

Priority

2. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-22 of this application. For example, the provisional application lacks support for all the features recited in independent claim 1, such as a wirebond pad, a circuit including an analog circuit and a digital circuit, and a switching circuit that selectively connects at least one of the analog input, analog output, digital input, and digital output to the wirebond pad under control of the processor.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,356,958 to Lin.

With regard to claim 1, Lin discloses a microcontroller including: a circuit including an analog circuit (Fig. 3, item 306) and a digital circuit, (Fig. 3, item 304 or 306) where the analog circuit includes an analog input and an analog output (Fig. 3, items 312 and 374) and the digital circuit includes a digital input and a digital output (Fig. 3, items 386, 376, and 388); a wirebond pad (Fig. 3, items 344, 324, and 340); a processor (Fig. 3, items 348, 356, and 364); and a switching circuit (Fig. 3, items 310) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the wirebond pad under control of the processor.

As shown in Fig. 3, the switching circuit 310 is controlled by the processors 348, 356, and 364 through select signals 1S, CS and OS. Based on the select signals, the switching circuit 310 selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the wirebond pad.

With regard to claim 3, Lin discloses the apparatus where the digital circuit includes a configurable digital circuit block (column 7, lines 6-8).

Therefore, Lin reads on the invention as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,509,758 to Piasecki, et al. ("Piasecki") in view of *Wirebonding: Reinventing the Process for MCMs* by H.K. Charles, et al. ("Charles").

With regard to claim 1, Piasecki discloses a microcontroller including: a circuit including an analog circuit (Fig. 1, item 22; column 3, lines 39-42) and a digital circuit, (Fig. 1, item 18) where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (*see generally*, Fig. 1 and column 3, lines 39-42); a pad (Fig. 1, item 12); a processor (Fig. 1, item 18); and a switching circuit (Fig. 1, items 14) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the pad under control of the processor (column 3, lines 31-33 and lines 54-59).

With regard to claims 17-21, Piasecki discloses the apparatus where the switching circuit includes a tristate logic gate coupling the digital input to the pad, and

where the digital input is switched by tristate control of the tristate logic gate; where the tristate logic gate includes an inverter; where the tristate logic gate includes a buffer; and where the multiple input logic gate includes a NAND gate (*see generally*, Fig. 2 and the accompanying text).

Piasecki does not expressly disclose a wirebond pad, as recited in independent claim 1. Charles discloses the use of wirebonding. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the wirebonding of Charles with the pad of Piasecki. The suggestion or motivation for doing so would have been to increase quality and reliability of the pads (page 300, paragraph 1, lines 5-8).

Therefore, it would have been obvious to combine Charles with Piasecki to obtain the invention as specified in claims 1 and 17-21.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,734,334 to Hsieh, et al. ("Hsieh") in view of Charles.

With regard to claim 1, Hsieh discloses a microcontroller including: a circuit including an analog circuit and a digital circuit, where the analog circuit includes an analog input and an analog output and the digital circuit includes a digital input and a digital output (*see generally*, column 3, lines 27-63); a pad (Fig. 1, items I0-I159 and/or items T0-T159); a processor (Fig. 1, item 16); and a switching circuit (Fig. 1, item 12) that selectively connects at least one of the analog input, the analog output, the digital input, and the digital output to the pad under control of the processor (column 3, lines 13-63).

Hsieh does not expressly disclose a wirebond pad, as recited in independent claim 1. Charles discloses the use of wirebonding. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the wirebonding of Charles with the pad of Hsieh. The suggestion or motivation for doing so would have been to increase quality and reliability of the pads (page 300, paragraph 1, lines 5-8).

Therefore, it would have been obvious to combine Charles with Hsieh to obtain the invention as specified in claim 1.

8. Claims 2 and 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 5,107,146 to El-Ayat.

As described above with regard to the 35 U.S.C. 102(e) rejection of independent claim 1, Lin discloses all the features of claim 1. Lin does not expressly disclose all the features of dependent claims 2 and 7-22.

El-Ayat discloses the features of claims 2 and 7-22. For example, El-Ayat discloses an apparatus where the analog circuit includes a configurable analog circuit block (column 1, lines 17-25). El-Ayat also discloses the apparatus where the switching circuit includes an analog buffer amplifier (Fig. 1, items 22a, 22b, 22c, and 22d) in series with an analog switch (Fig. 1, item 24) coupling the analog output to the pads (Fig. 1, items 18e, 18f, 18g, and 18h), and where the analog output is switched by the analog switch; where the switching circuit includes an analog switch (Fig. 1, item 24) coupling the analog output to the pads (Fig. 1, items 18e, 18f, 18g, and 18h), and where the analog output is switched by the analog switch; and where the switching circuit

includes an analog switch (Fig. 1, item 24) coupling the analog input (Fig. 1, items 20a, 20b, 20c, and 20d) to the pads (Fig. 1, items 18a, 18b, 18c, and 18d), and where the analog input is switched by the analog switch.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine El-Ayat with Lin. The suggestion or motivation for doing so would have been to isolate the switch from the effects of the pads, and vice versa; and to provide more flexibility such that the user can selectively change the configuration of the analog circuit.

Therefore, it would have been obvious to combine El-Ayat with Lin to obtain the invention as specified in claims 2 and 7-22.

Response to Arguments

9. Applicant's arguments filed November 4, 2004 with regard to priority have been fully considered but they are not persuasive.

None of Applicant's cited text from the provisional application discloses a "wirebond pad" or the connection to a "wirebond pad" as claimed.

Therefore, the Examiner cannot agree that domestic priority should be granted.

10. Applicant's arguments filed November 4, 2004 with regard to the 35 USC 102(e) rejections of claims 1 and 3 as being anticipated by Lin have been fully considered but they are not persuasive.

On page 13, Applicant argues that Lin does not teach a microcontroller where "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by the switching circuit to the wirebond pad" as recited in claim 1. Contrary to Applicant's arguments, Lin does disclose this feature. For example, in Fig. 3, at least one of the analog input, the analog output, the digital input and the digital output is selectively connected to the wirebond pad. As claimed, the switching circuit 310 is controlled by the processors 348, 356, and 364 through select signals 1S, CS and OS.

Furthermore, Applicant argues that Lin "teaches away" from the invention as claimed because the Abstract discloses "[t]he selectable functions are selected during packaging of the known good integrated circuit die." Applicant is reminded that the question of whether a reference "teaches away" from the invention is inapplicable to an anticipation analysis. *Celeritas Technologies Ltd. v. Rockwell International Corp.*, 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir.1998) (The prior art was held to anticipate the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed."). See also *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999) (Claimed composition was anticipated by prior art reference that inherently met claim limitation of "sufficient aeration" even though reference taught away from air entrapment or purposeful aeration.). *See* MPEP 2131.05.

In response to Applicant's argument that the Lin fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., selectively connecting functionality at any time after packaging and user-configurable functionality) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the Examiner cannot allow claims 1 and 3.

11. Applicant's arguments filed November 4, 2004 with regard to the 35 103 USC(a) rejection of claims 1 and 17-21 as being unpatentable over Piasecki in view of Charles have been fully considered but they are not persuasive.

In response to Applicant's argument that the Piasecki reference fails to show certain features of Applicant's invention, it is noted that the features upon which applicant relies (i.e., dedicated pins for analog input and analog output, and dedicated pins for digital input and digital output) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, on page 14, Applicant argues that neither Piasecki nor Charles teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor" as claimed. Contrary to Applicant's assertion, Piasecki in view of Charles does teach this feature. For example, in Fig. 1, the digital output from

digital circuit 18 is selectively connected to the pad 12 by the switching circuit 14 (*see generally*, column 3, lines 50-67 to column 5, lines 1-24). As claimed, processor 18 controls the switching circuit 14 via control signals from the control register 28 (*see* column 3, lines 31-33 and lines 54-59).

Therefore, the Examiner cannot allow claims 1 and 17-21.

12. Applicant's arguments, see pages 14-16, filed November 4, 2004, with respect to the rejections of claim 1 under 35 USC 103(a) as being unpatentable over Calloway in view of Charles and as obvious over Fornek in view of Charles have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Hsieh.

The Examiner is persuaded that neither Calloway nor Fornek expressly disclose a pad, as claimed. However, Hsieh teaches this feature, and Hsieh in view of Charles teaches the use of a wirebond pad, as claimed.

Therefore, the Examiner cannot allow claims 1.

13. Applicant's arguments, see pages 16-17, filed November 4, 2004, with respect to the rejection of claim 2 under 35 USC 103(a) as being unpatentable over Lin in view of Kohno have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of El-Ayat.

The Examiner is persuaded that Applicant's U.S. filing date of June 26, 2001 has priority over the Kohno U.S. Filing date of August 19, 2002. Therefore, Kohno is not prior art. However, upon further review of El-Ayat, the Examiner finds that El-Ayat teaches the features of claim 2.

Therefore, the Examiner cannot allow claim 2.

14. Applicant's arguments, filed November 4, 2004, with regard to the 35 USC 103(a) rejection of claims 7-22 as being unpatentable over Lin in view of El-Ayat have been fully considered but they are not persuasive.

On pages 17-18, Applicant argues Lin fails to teach or suggest "a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor" as claimed in claim 1. However, as discussed above, Lin teaches this feature.

Furthermore, Applicant argues that El-Ayat teaches away from the claimed invention because it discloses analog-to-digital and digital-to-analog converters. However, as shown in Fig. 1, El-Ayat discloses analog circuits 12a-12d and digital circuits 14a-14f. By way of switch 24, at least one of the analog input, the analog output, the digital input, and the digital output is selectively connected to pads 18a-18h. In this way, El-Ayat does not teach away from the invention.

Therefore, the Examiner cannot allow claims 7-22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (571) 272-3629. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

TIM VO
PRIMARY EXAMINER